IN THE CLAIMS

1-26. (Canceled)

27. (New) A semiconductor integrated circuit device comprising:

a first circuit block including a plurality of first logic gates and second logic gates; and

a second circuit block including a plurality of first logic gates and second logic gates,

wherein the first logic gates include a first MOSFET having a first threshold voltage and the second logic gates include a second MOSFET having a second threshold voltage higher than the first threshold voltage,

wherein a process condition of the first MOSFET is different from a process condition of the second MOSFET so that the first threshold voltage is different from the second threshold voltage, and

wherein ratio number of the first logic gates included in the first circuit block to number of all logic gates in the first circuit block is higher than ratio number of the first logic gates included in the second circuit block to number of all logic gates in the second circuit block.

28. (New) The semiconductor integrated circuit device according to claim 27,

wherein the first circuit block is one of a central processing unit, floating unit processing unit and cache and the second circuit block is an interrupt control circuit .

29. (New) The semiconductor integrated circuit device according to claim 27,

wherein an impurity density of an area formed the second MOS transistor thereon is higher than an impurity density of an area formed the first MOS transistor thereon.

30. (New) The semiconductor integrated circuit device according to claim 27,

wherein a gate insulation film of the second MOS transistor is thicker than a gate insulation film of the first MOS transistor.

31. (New) The semiconductor integrated circuit device according to claim 27,

wherein a gate length of the second MOS transistor is longer than a gate length of the first MOS transistor.